Design Challenges of Next-Generation Wireless Communication SoCs

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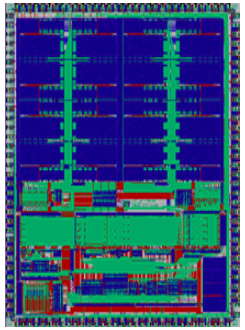
Communication SoC Technologies

- Lots of innovations and new ideas in communication signal processing
  - W-CDMA, DFE, OFDM, antenna beam-forming, MIMO, etc.
- What makes an algorithm appropriate for implementation is rapidly changing
  - Digital computation exponentially improving
  - Complex analog circuits linearly degrading (?)
- Power dissipation has become one of the main showstoppers.

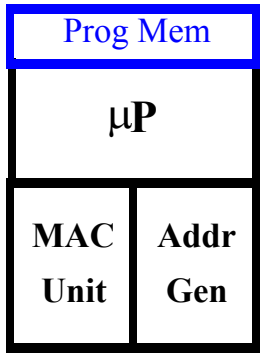
Requires 100's of GOP's of processing per device - how to do it at the lowest energy and smallest area???

Energy and Area Efficiency

0.5-5 MIPS/mW
10 MIPS/mm²

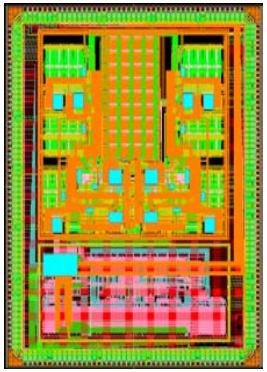


Embedded Processor (ARM)



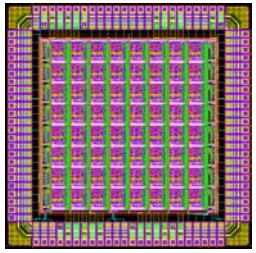
DSP

10-100
MOPS/mW

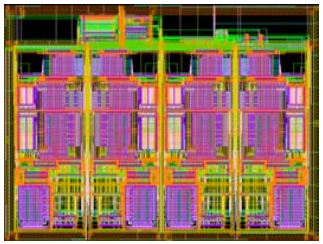


Reconfigurable Processors

1000 MOPS/mW
1000 MOPS/mm²



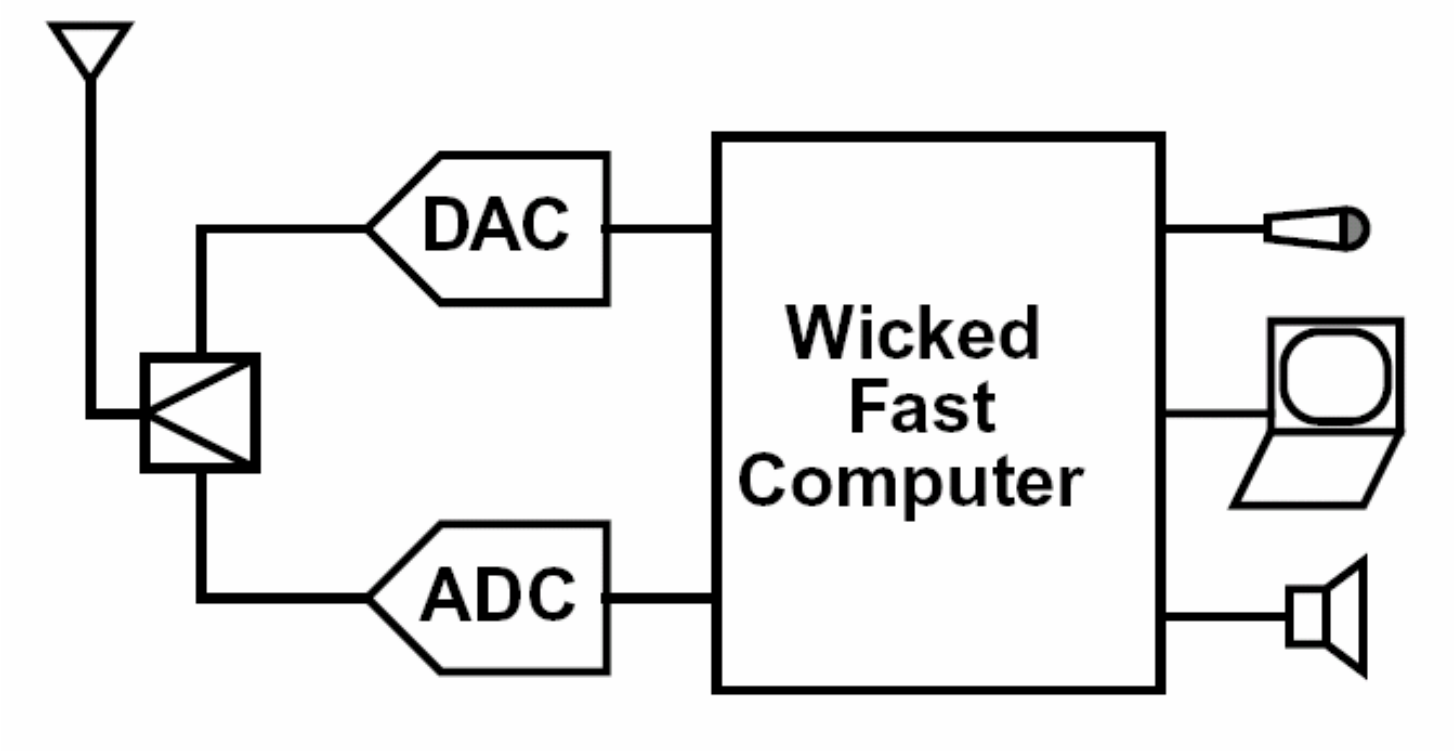
Embedded FPGA



Direct Mapped Hardware

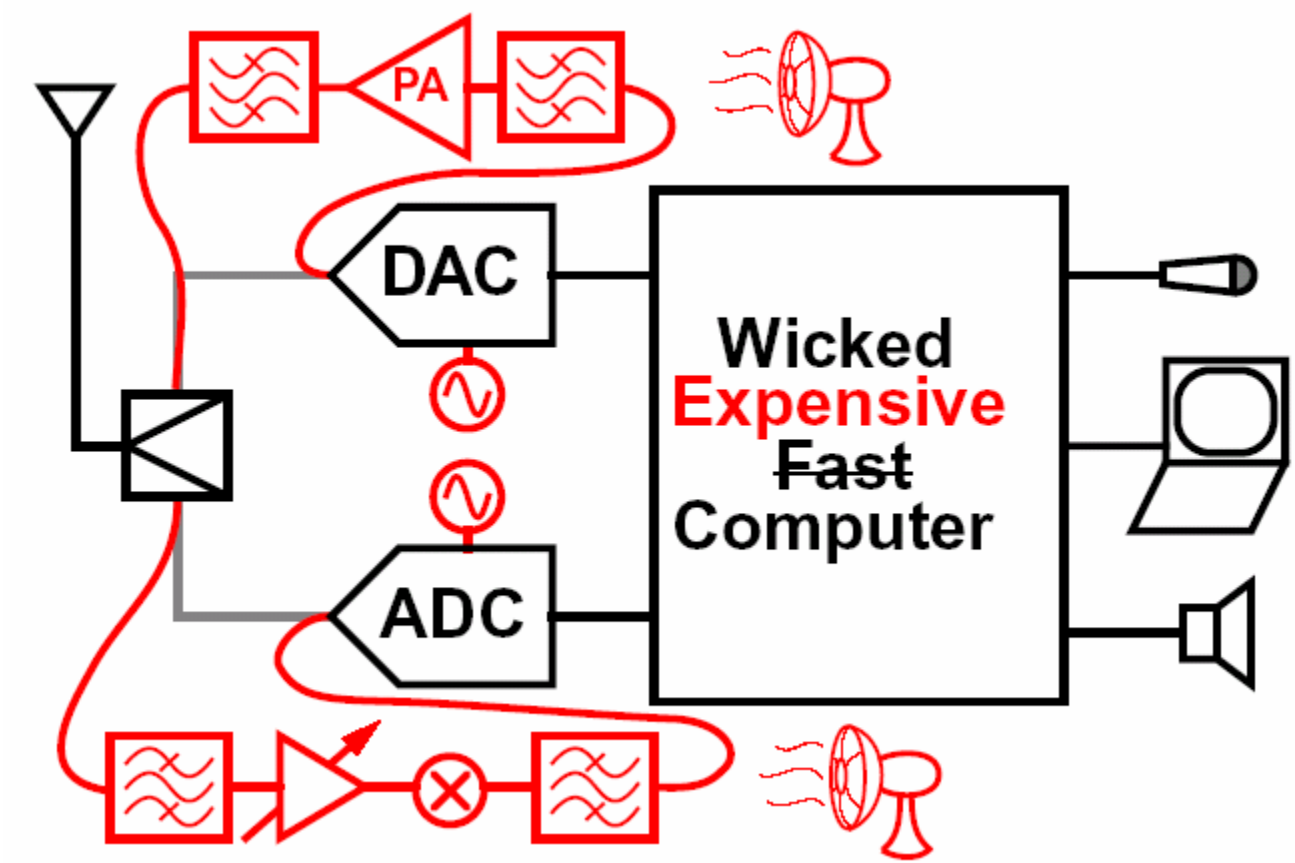
Factor of 100-1000

The Dream – "Software Radio"



[Schreier, "ADCs and DACs: Marching Towards the Antenna," GIRAFE workshop, ISSCC 2003]

Reality – "Heat-sink Radio"



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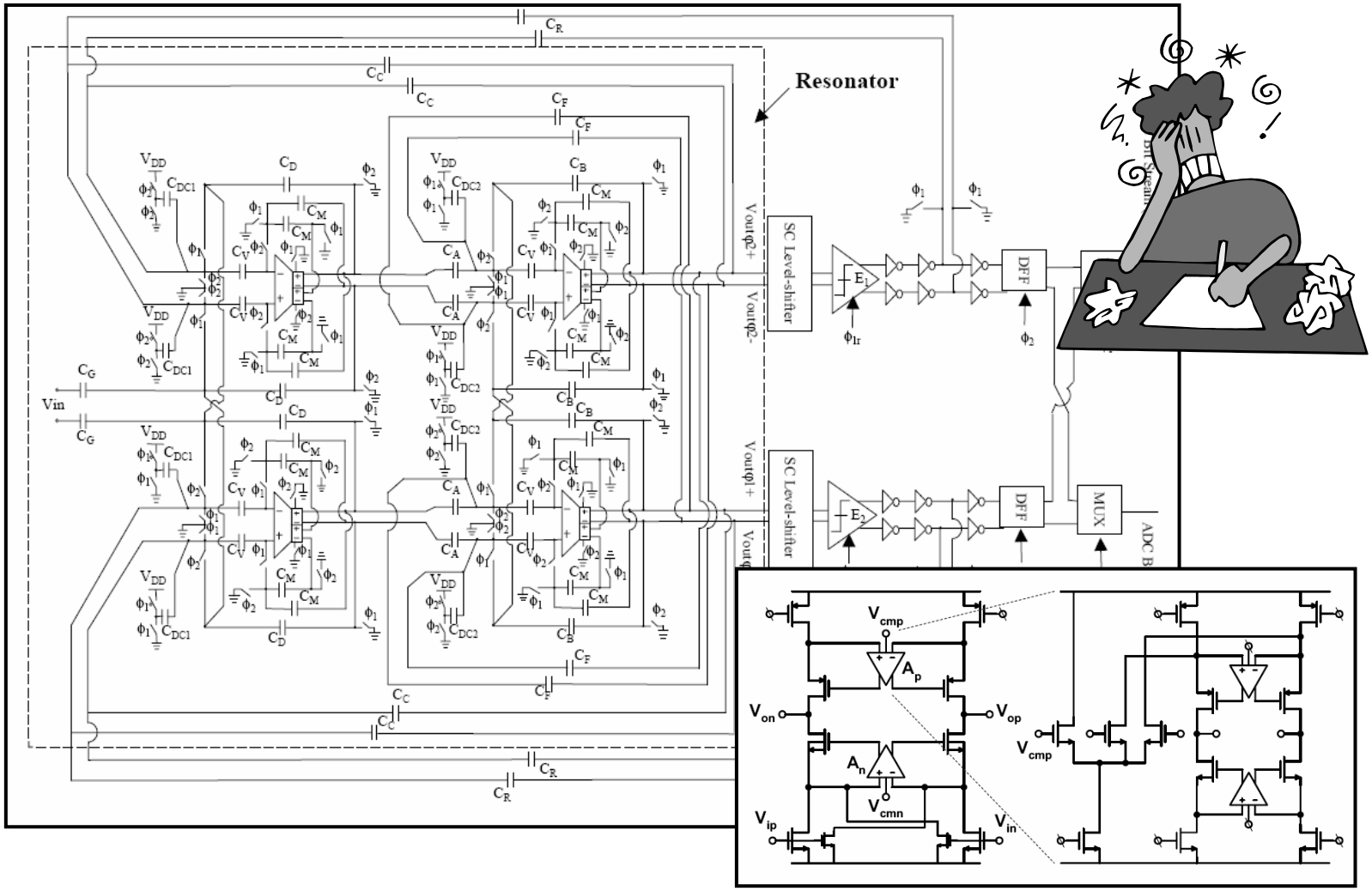
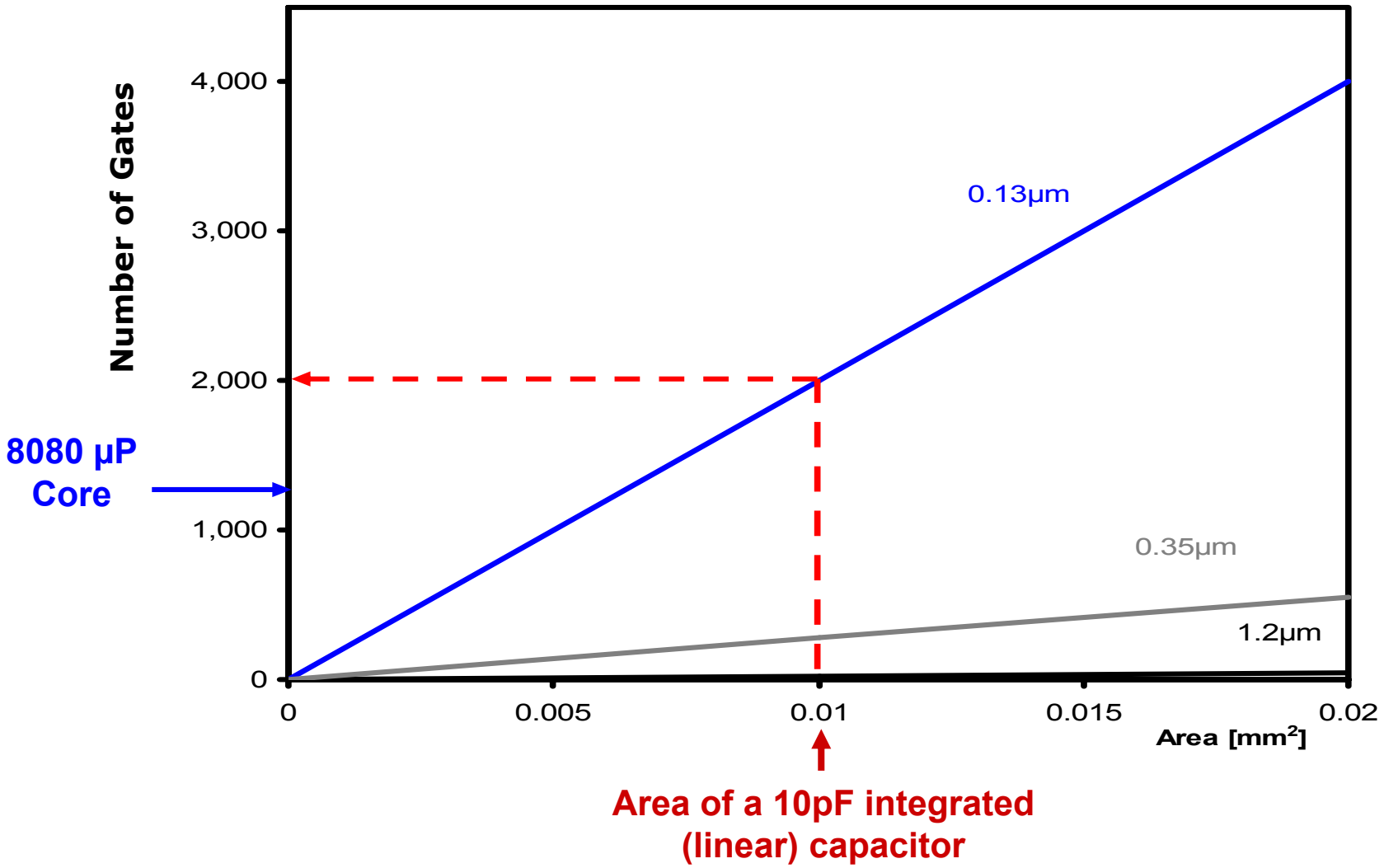
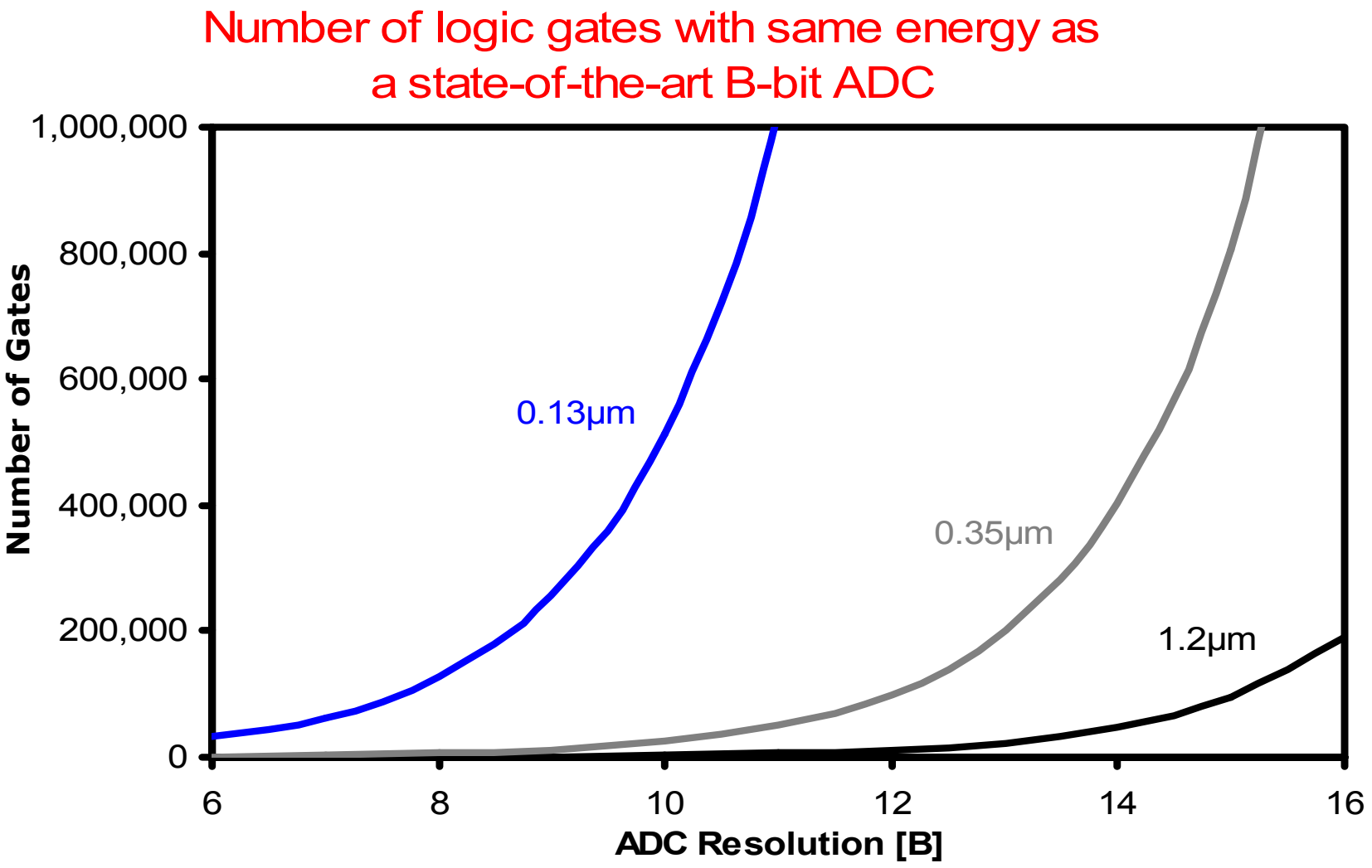
Today's Analog Circuits



Digital Density vs. Analog Area

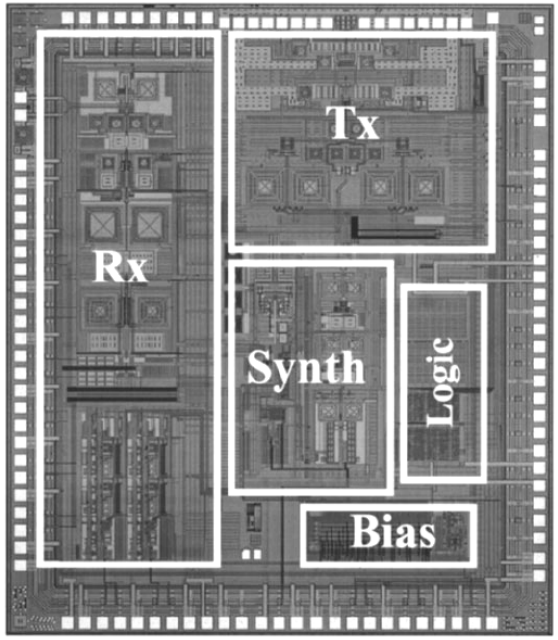


Digital Energy Efficiency



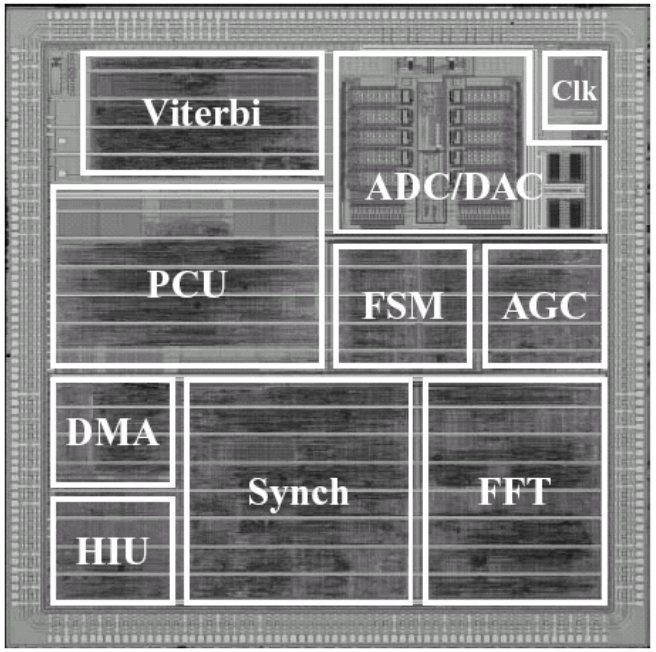
Real Life Example: 802.11 a/g

RF



Rx ~ 300mW
Tx ~ 1500mW

Baseband



Digital (50 GOPS, 0.13μm) ~ 50mW
ADC (2x9b, 80MHz) ~ 200mW

Observations

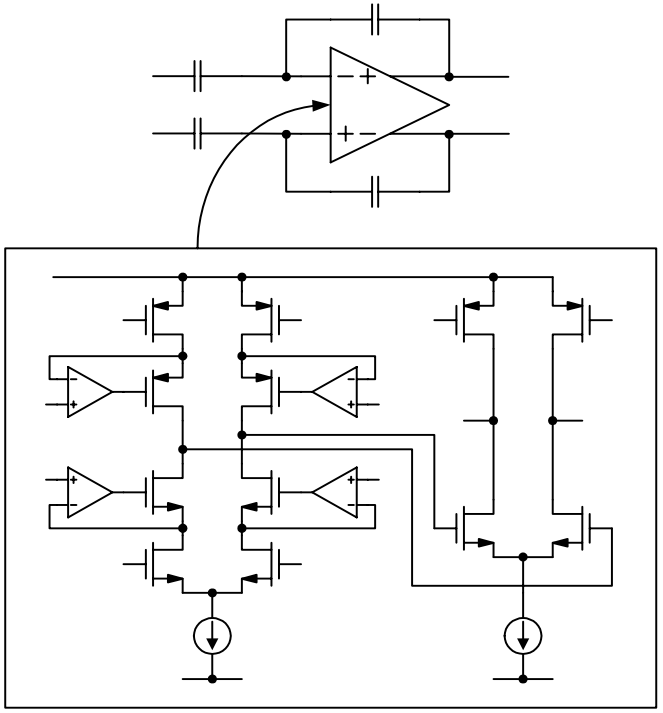
- It is not new to realize that digital signal processing is superior to analog in terms of energy efficiency
- What's new is the relative size of the gap between digital and analog capabilities, mostly due to advancements of last 10 years
- Necessary paradigm shift
  - Today: "Let's use some logic gates to correct/calibrate analog circuits"
  - Future: "How many analog transistors do we really need?"
- How can we use digital logic more aggressively to "assist" analog functions, such as ADCs and PAs?

Analog Circuit Challenges

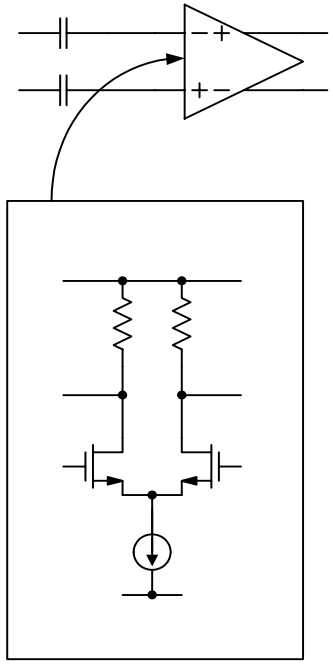
- Thermal Noise
  - Set by supply voltage and capacitance
  - Fundamental
- Distortion
  - Exacerbated by low supplies & intrinsic device gain
  - Traditional solution: high-gain feedback
  - Not fundamental

Back to the Future

Precision Amplifier

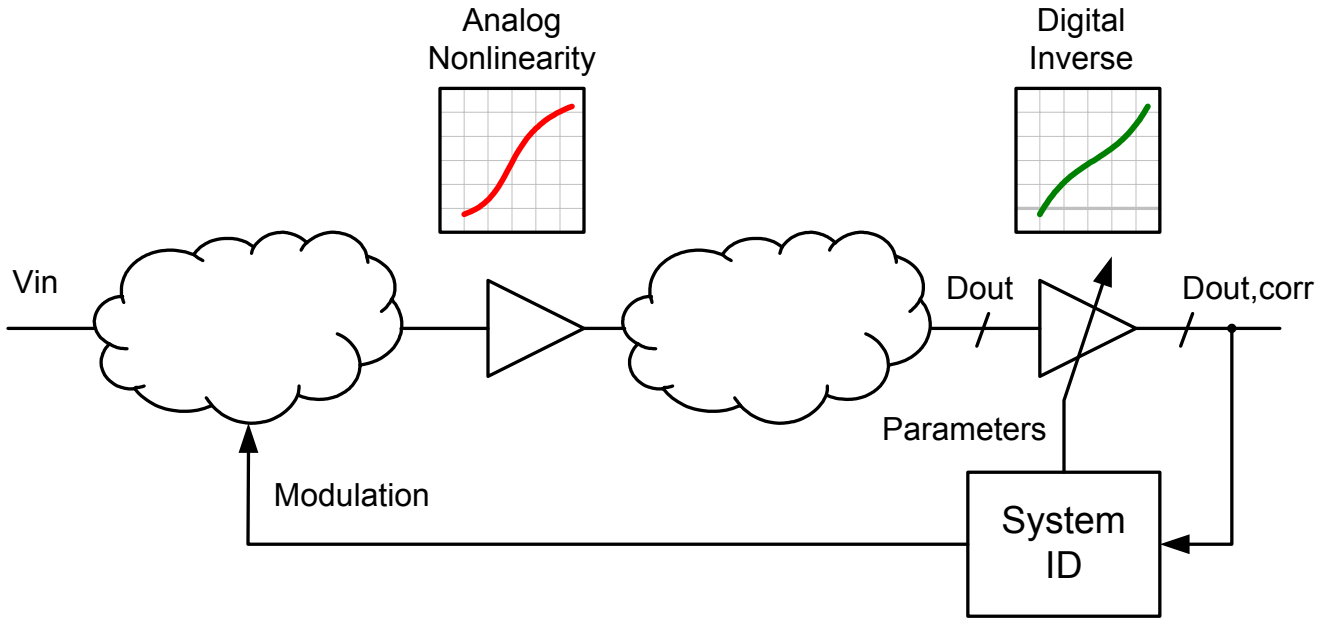


“Open loop“



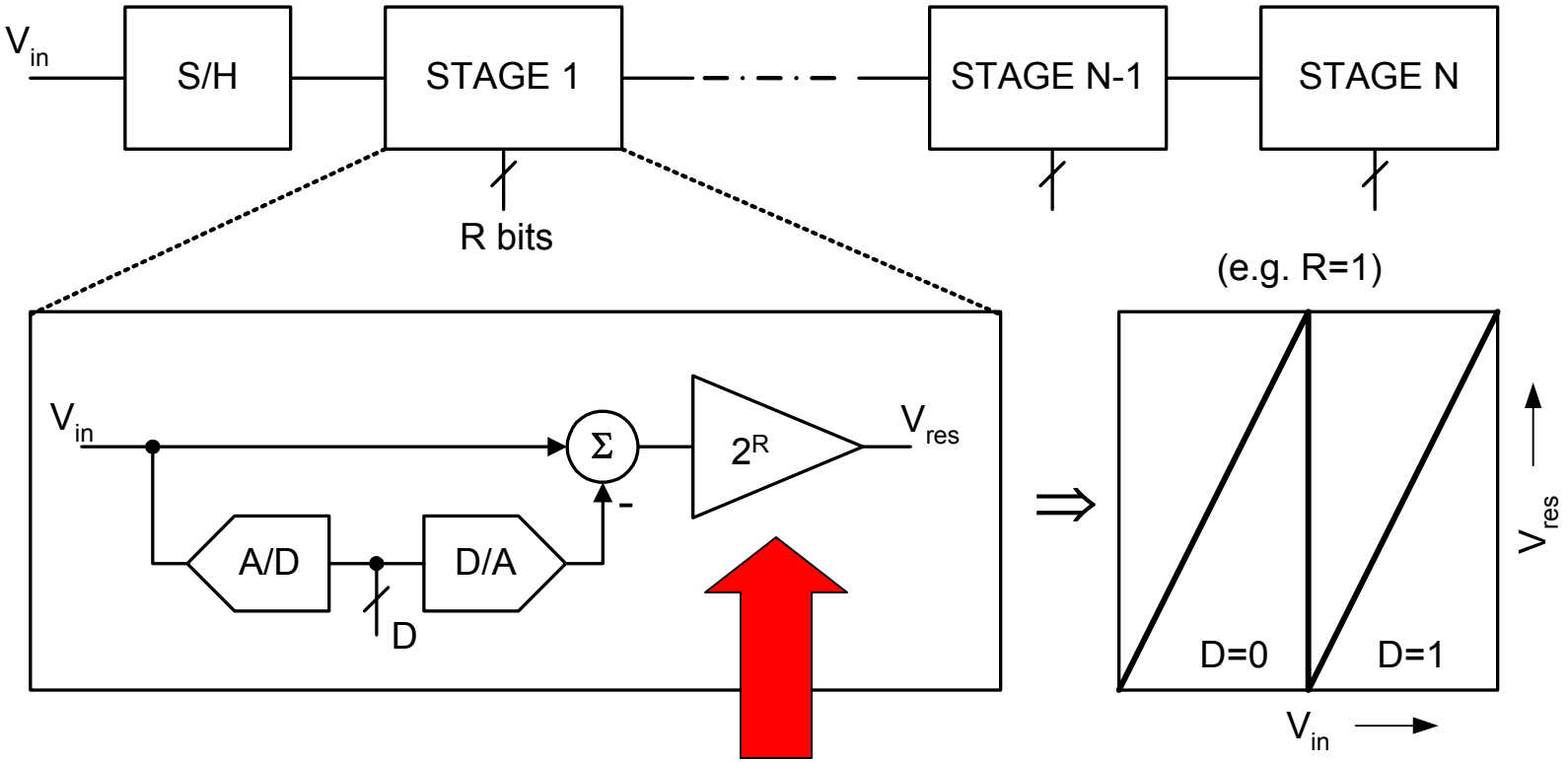
+ Lower Noise
+ Increased Signal Range
+ Lower Power
+ Faster
+ "Simple"
– Nonlinear
  - Use DSP to linearize!

Digital Nonlinearity Compensation

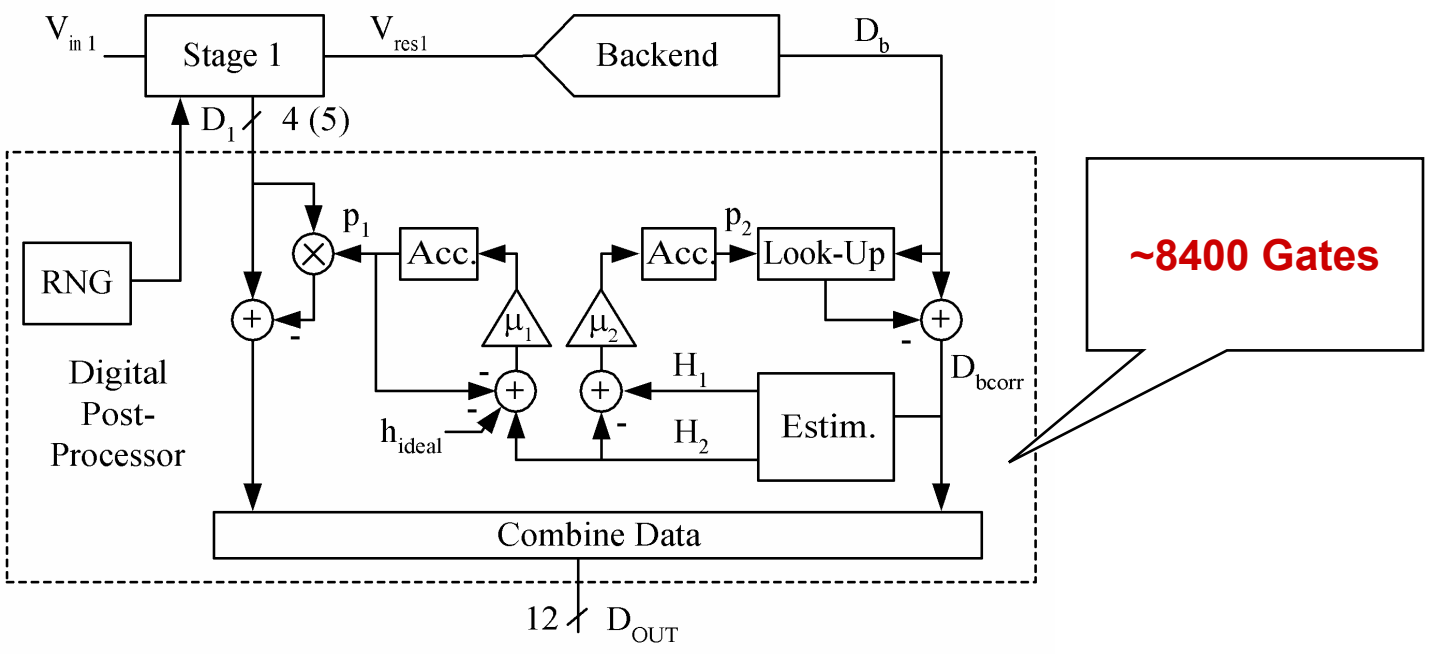


- Use system ID to determine optimum post correction
- Possible to track variations over time without interrupting normal circuit operation

Example: Pipelined ADC

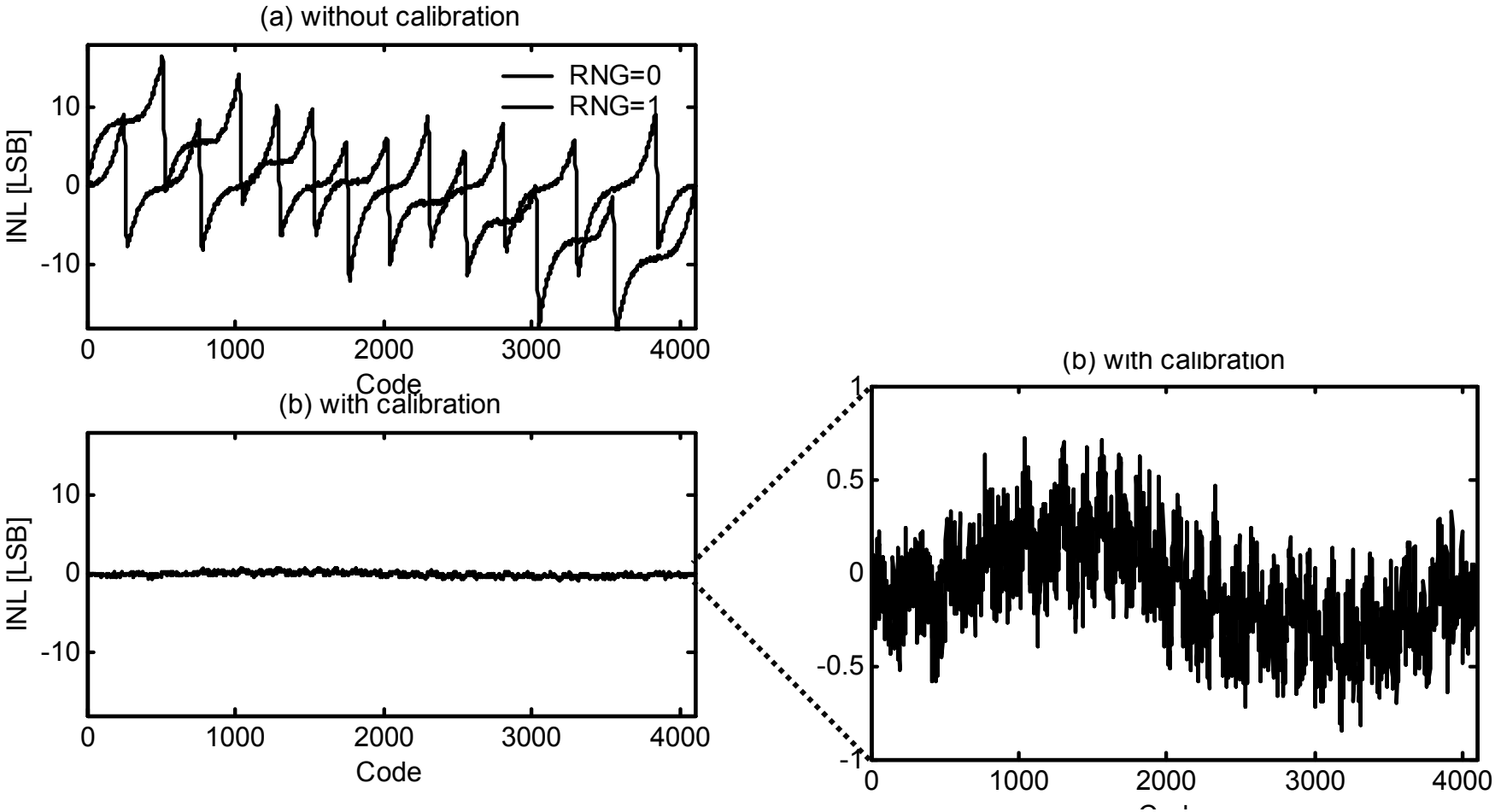


Block Diagram

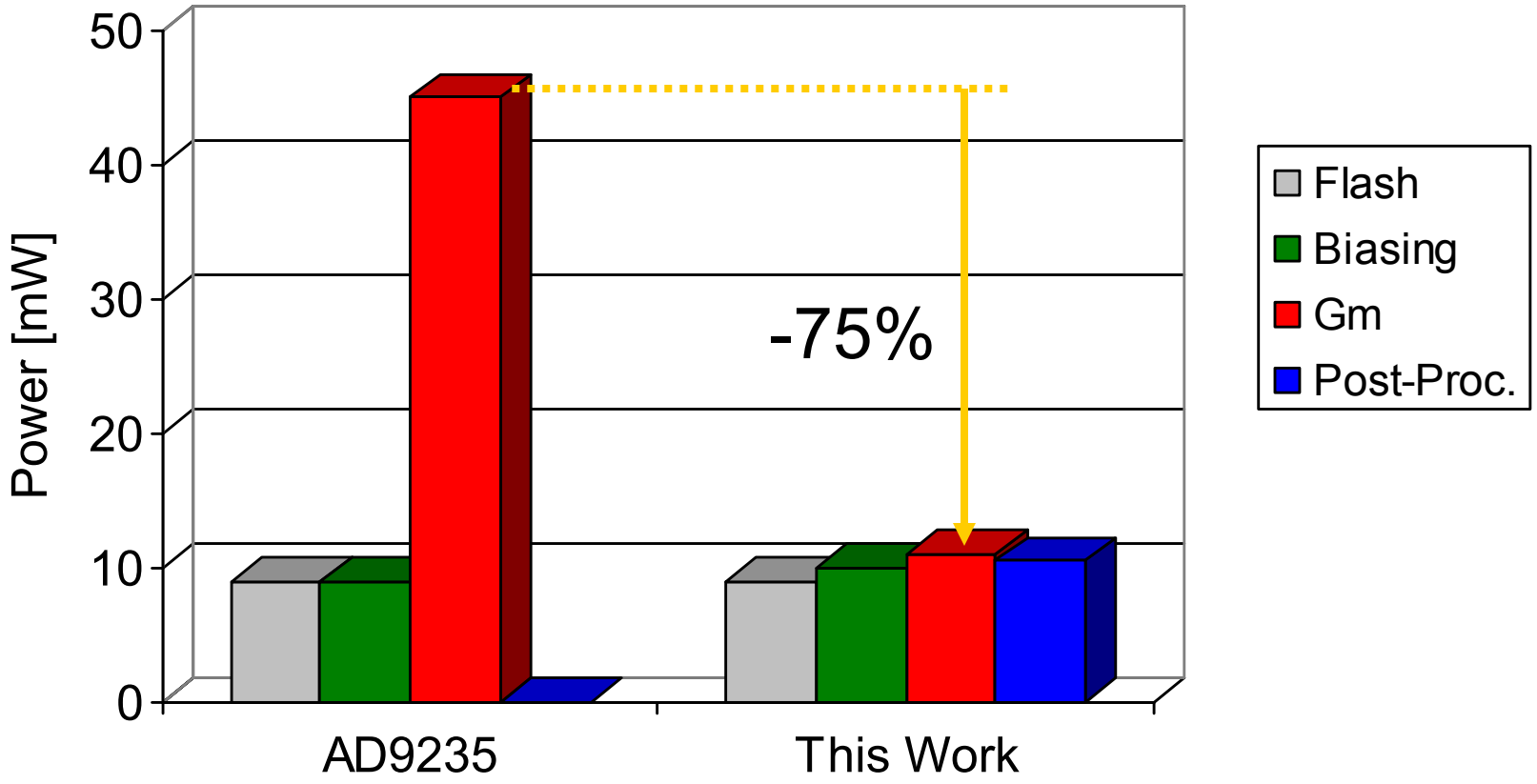


- Open-loop amplifier in the first, most critical stage
- Statistics based system ID allows continuous parameter tracking
- Judicious analog/digital co-design
  - Only two corretion parameters (linear and cubic error)

Measurement Results



Stage 1 Power Breakdown



Bottom Line

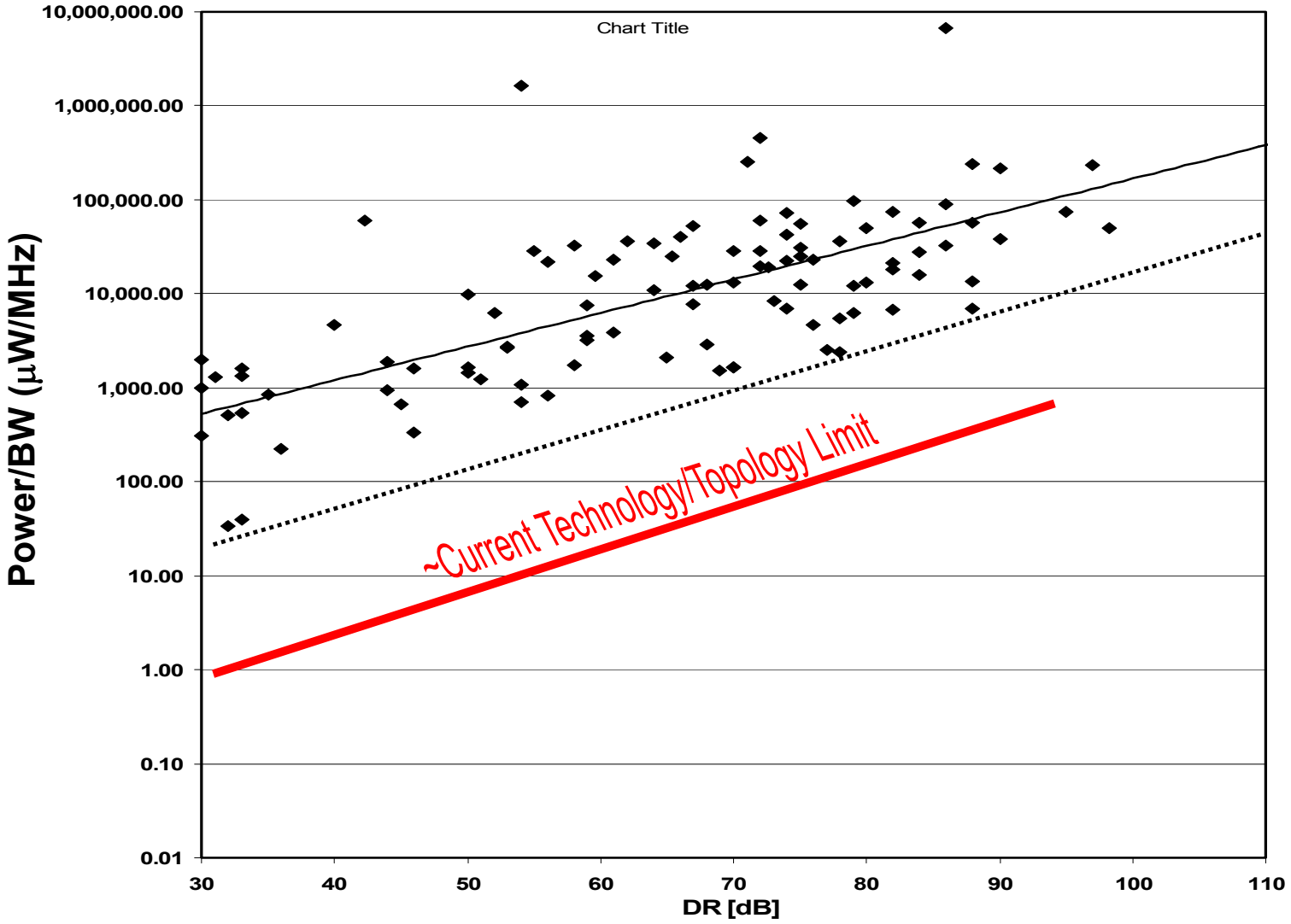


Chart Title
10,000,000.00
1,000,000.00
100,000.00
10,000.00
1,000.00
100.00
10.00
1.00
0.10
0.01
Power/BW (μW/MHz)
30
40
50
60
70
80
90
100
110
DR [dB]
~Current Technology/Topology Limit

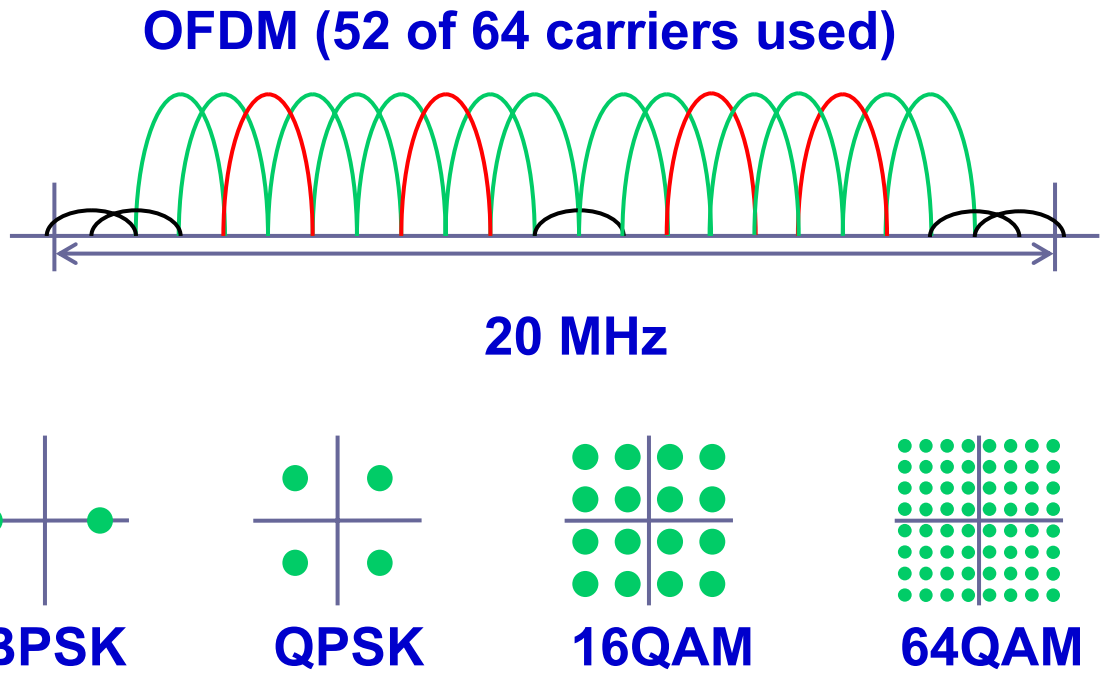
Summary - Digitially Assisted ADCs

- Simplified analog circuits are key to improving power efficiency in A/D
  - Power savings of better than one order of magnitude seem possible
- Other benefits of simplistic analog designs
  - Introduces redundancy, e.g. for yield enhancement
  - Creates adjustable, massively parallel arrays in small area
- Inherently self-calibrating, potentially self-repairing
  - Simplifies testing
  - Ideal for remote, maintenance free operation, e.g. in remote sensing networks

Digitally Assisted PA Design

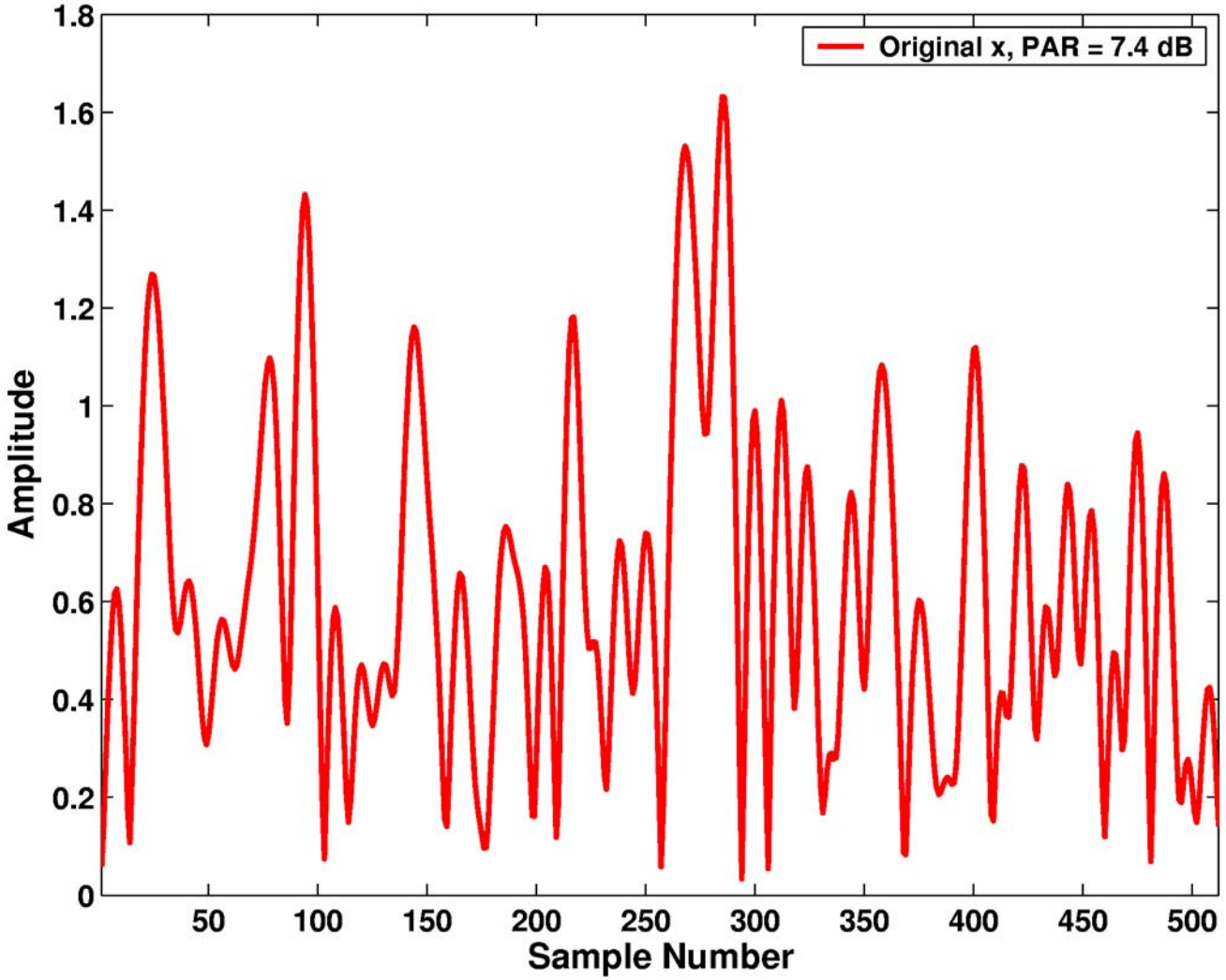
- Transmitter power efficiency is limited by
  - High peak-to-average power ratio (PAR)
  - Power amplifier (PA) non-linearity
- Linear PA design is increasingly difficult
- Digital circuit capabilities grow exponentially
  - 1 GOPS/mW, 1 GOPS/mm^2 in 0.13 μm CMOS
- How to achieve maximum power efficiency?

PA Design Example: 802.11a/g



- Of 64 the carriers:
  - 12 free carriers (in black) on sides and center
  - 48 data carriers (in green) per symbol
  - 4 pilots carriers (in red) per symbol for synchronization

High PAR in Time-domain Signal



Peak-to-average Power Ratio

- PAR of an OFDM symbol is

$$\mathrm{PAR} = \frac{\text{Peak time-domain power}}{\text{Average data-carrier power}}$$

- High PAR reduces power efficiency: 7.4 dB PAR ~ 10%
- May use free carriers but include only data-carrier power in the average
- Can express “minimize PAR” objective in convex form

Convex Optimization

- Standard Convex Optimization Problem

$$\begin{array}{ll} \text{minimize} & f_0(x) \\ \text{subject to} & f_i(x) \le 0 \quad i = 1, \mathrm{K}\ , m \\ & Ax = b \\ \text{in variables} & x \in \mathbf{R}^n \end{array}$$

- Each *f(x)* is a convex function

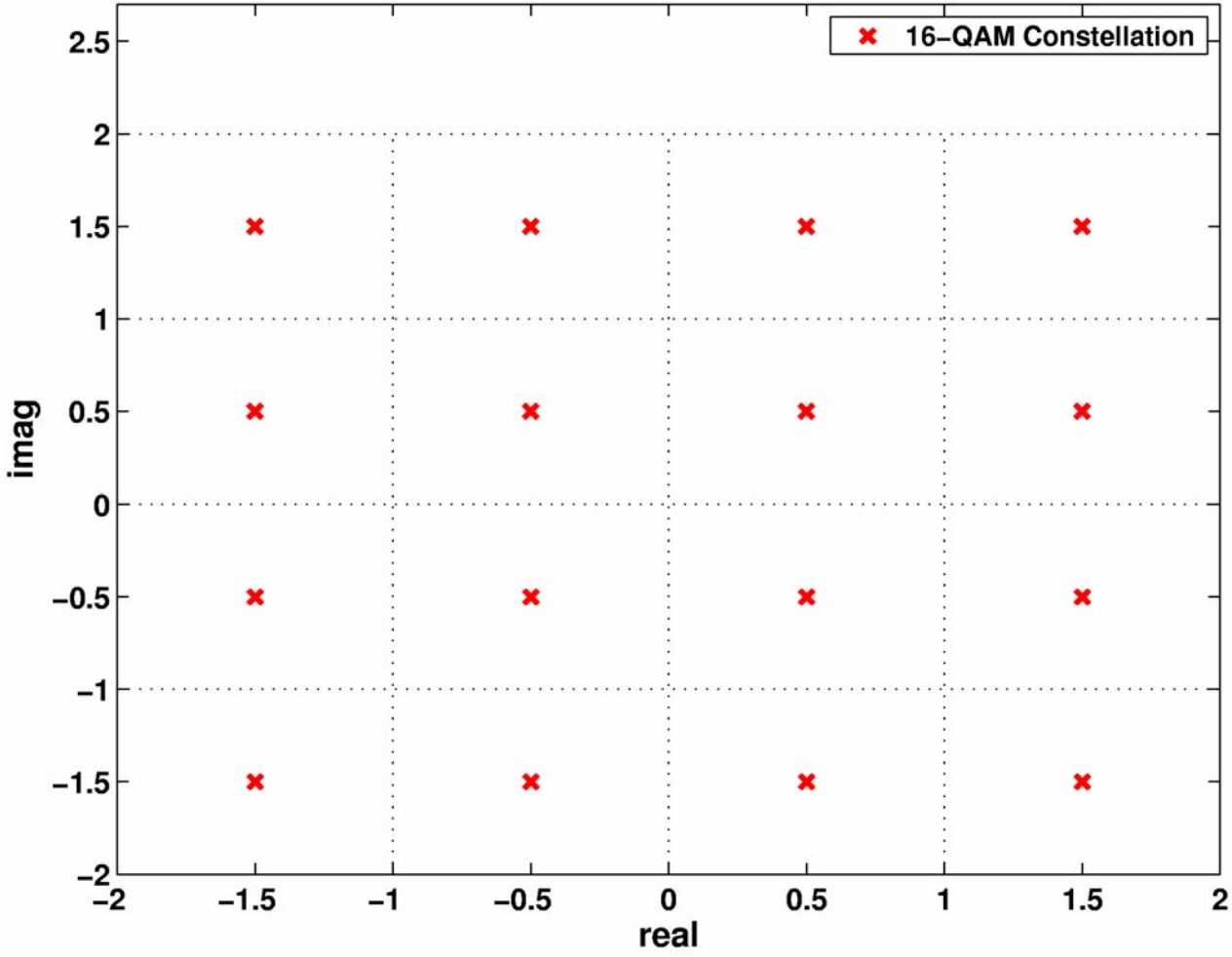
$$f(\theta x + (1-\theta)y) \le \theta f(x) + (1-\theta) f(y), \quad \text{for all } \theta \in [0,1]$$

- The globally optimal solution can be efficiently calculated
  - "The great watershed in optimization isn't between linearity and nonlinearity, but convexity and nonconvexity."

    --R. Rockafellar, SIAM Review, June 1993

Transmitter Constraints

- PAR reduction should not change receiver structure



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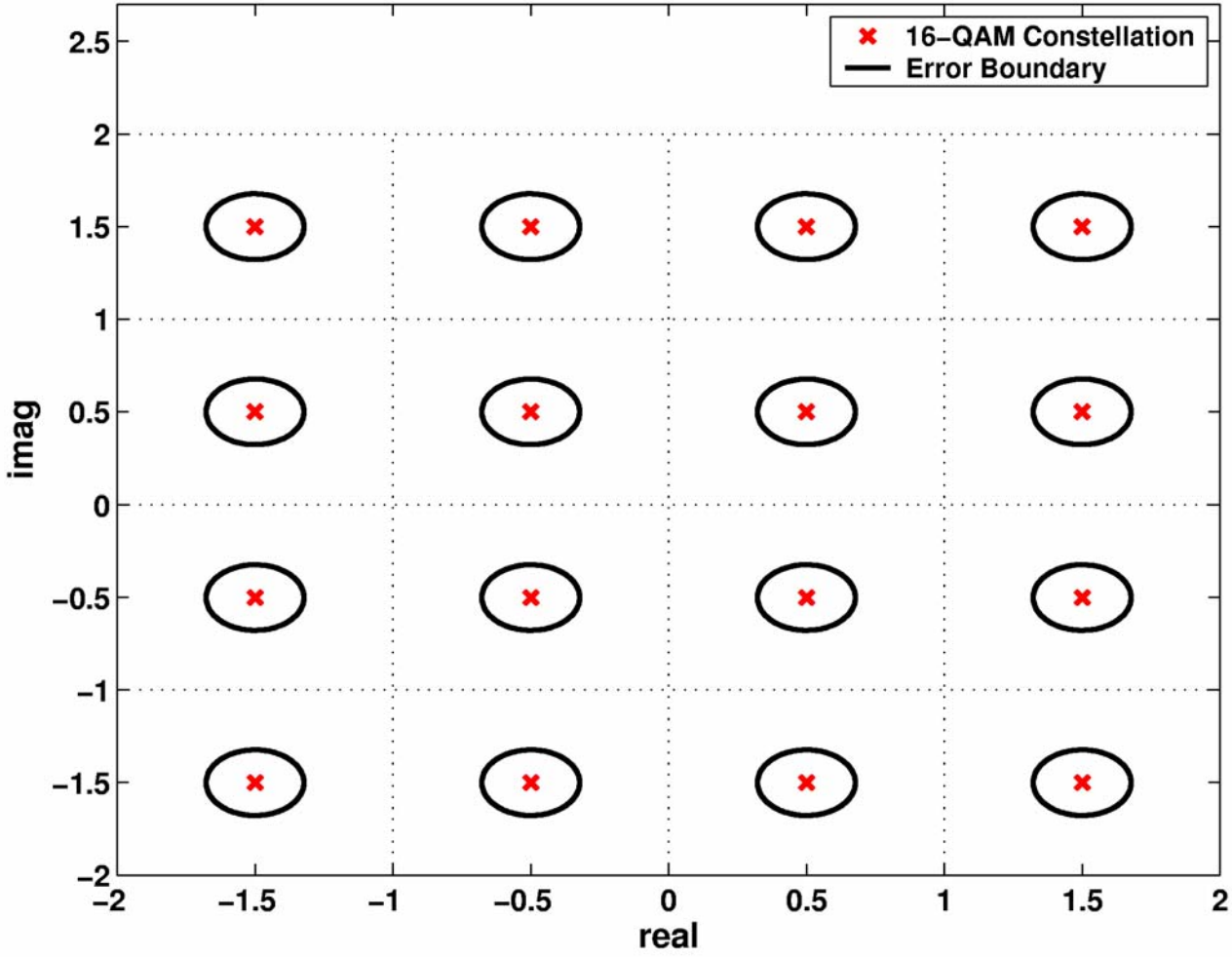


Transmitter Constraints

- Ideal OFDM constellation c, transmitted constellation ĉ
- Data carrier Error Vector Magnitude constraint
  - Limit individual EVM

$$\left\| \hat{c}_i - c_i \right\| \le \varepsilon, \quad i = i_1, i_2, \ldots, i_D$$

  - Limit average EVM

$$\sqrt{\frac{1}{D} \sum_{i=i_i}^{i_D} \left\| \hat{c}_i - c_i \right\|^2} \le \varepsilon$$

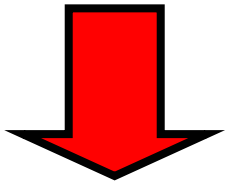
- Free carrier Spectral Mask constraint

$$\left\| \hat{c}_i \right\| \le \delta_i$$

- Constraints are convex inequalities

PAR Minimization

- PAR objective is convex
- Constellation constraints are convex



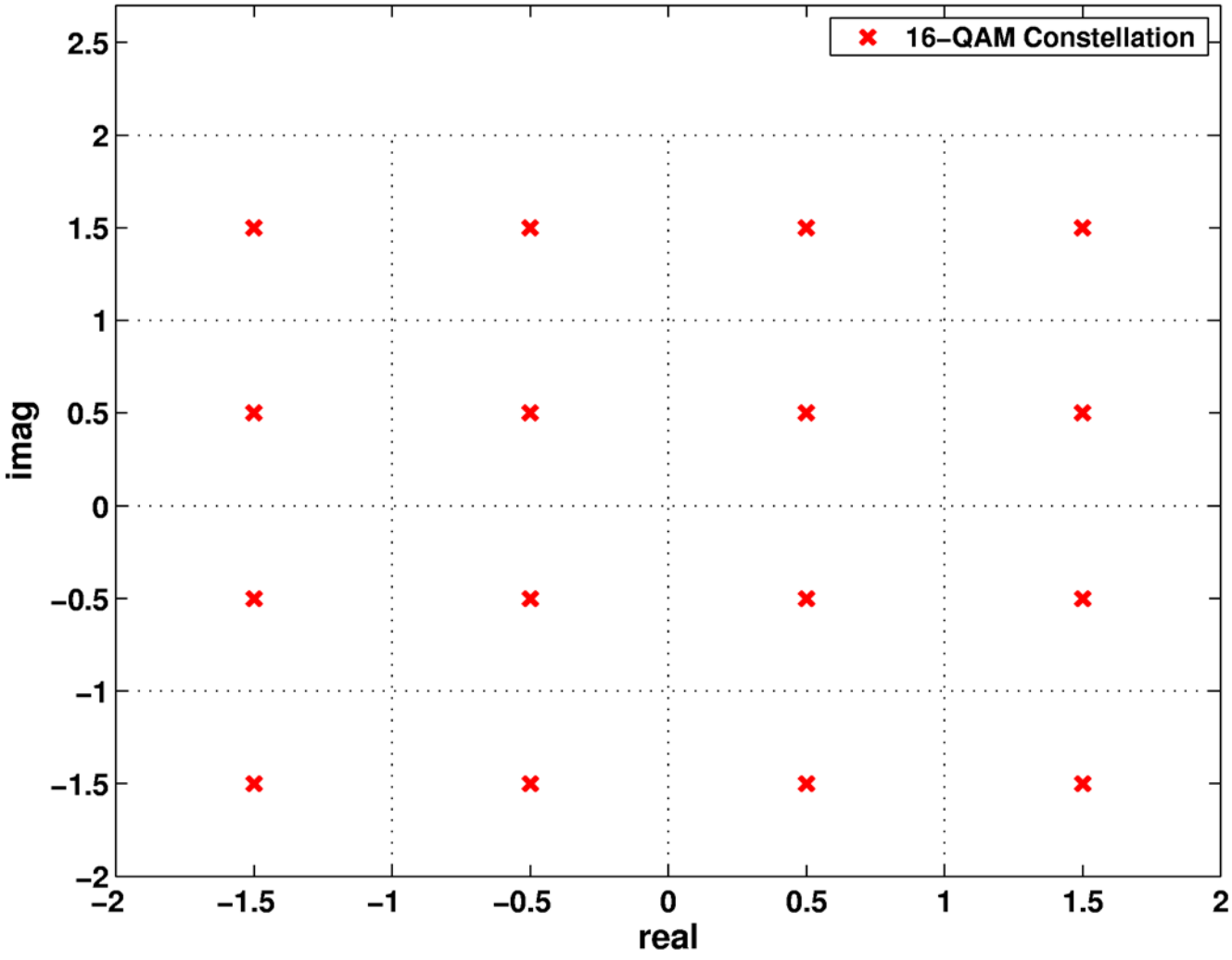
PAR minimization is a convex problem

- Use convex optimization theory to find the signal with MINIMUM PAR that satisfies transmitter EVM
- Controlled error vs. random error introduced in the constellation points in frequency domain

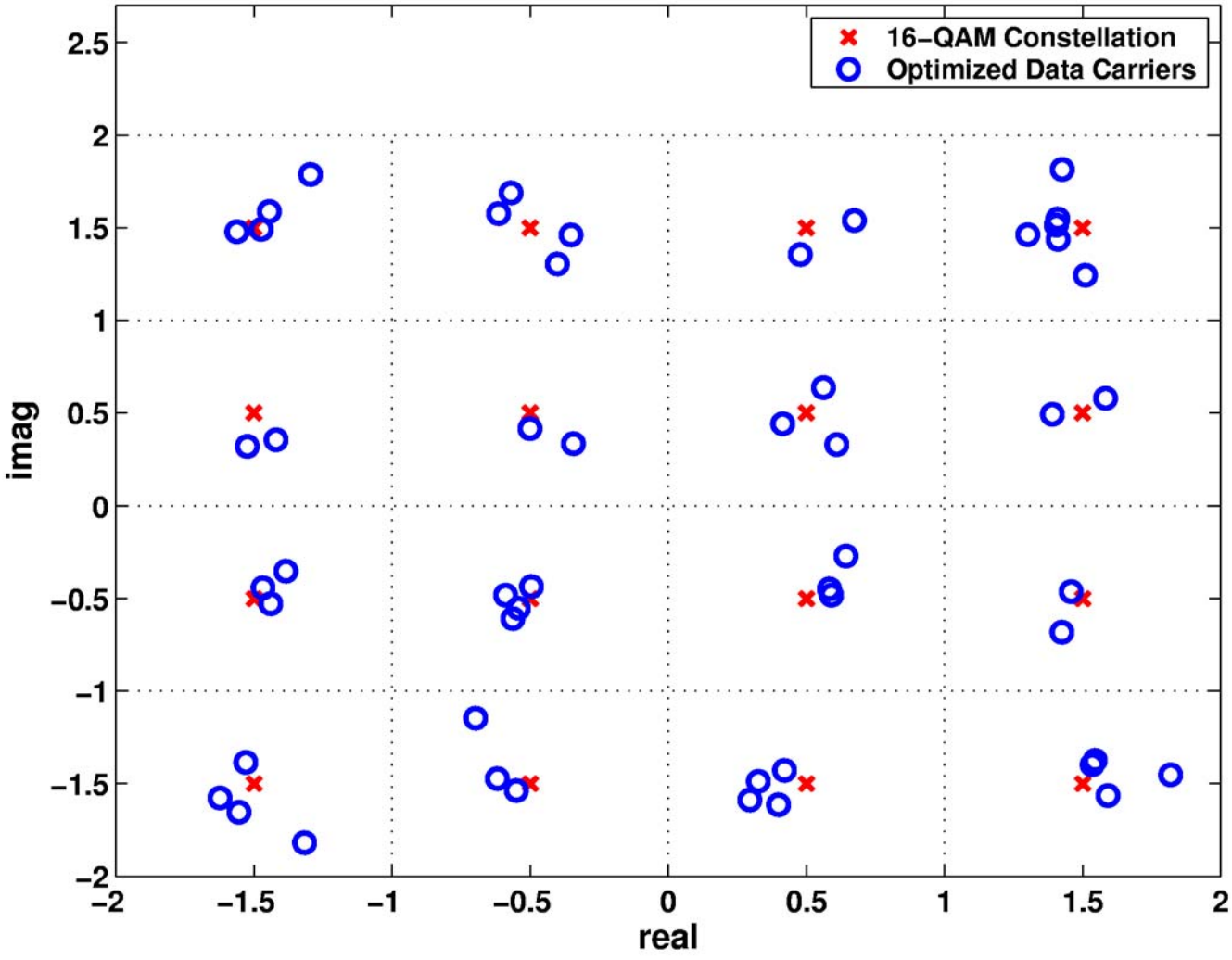
Optimization Example

- 802.11a/g WLAN standard
  - 52 data carriers
  - 12 free carriers
- Consider a random OFDM symbol
  - 16-QAM
  - Maximum average EVM = -19 dB

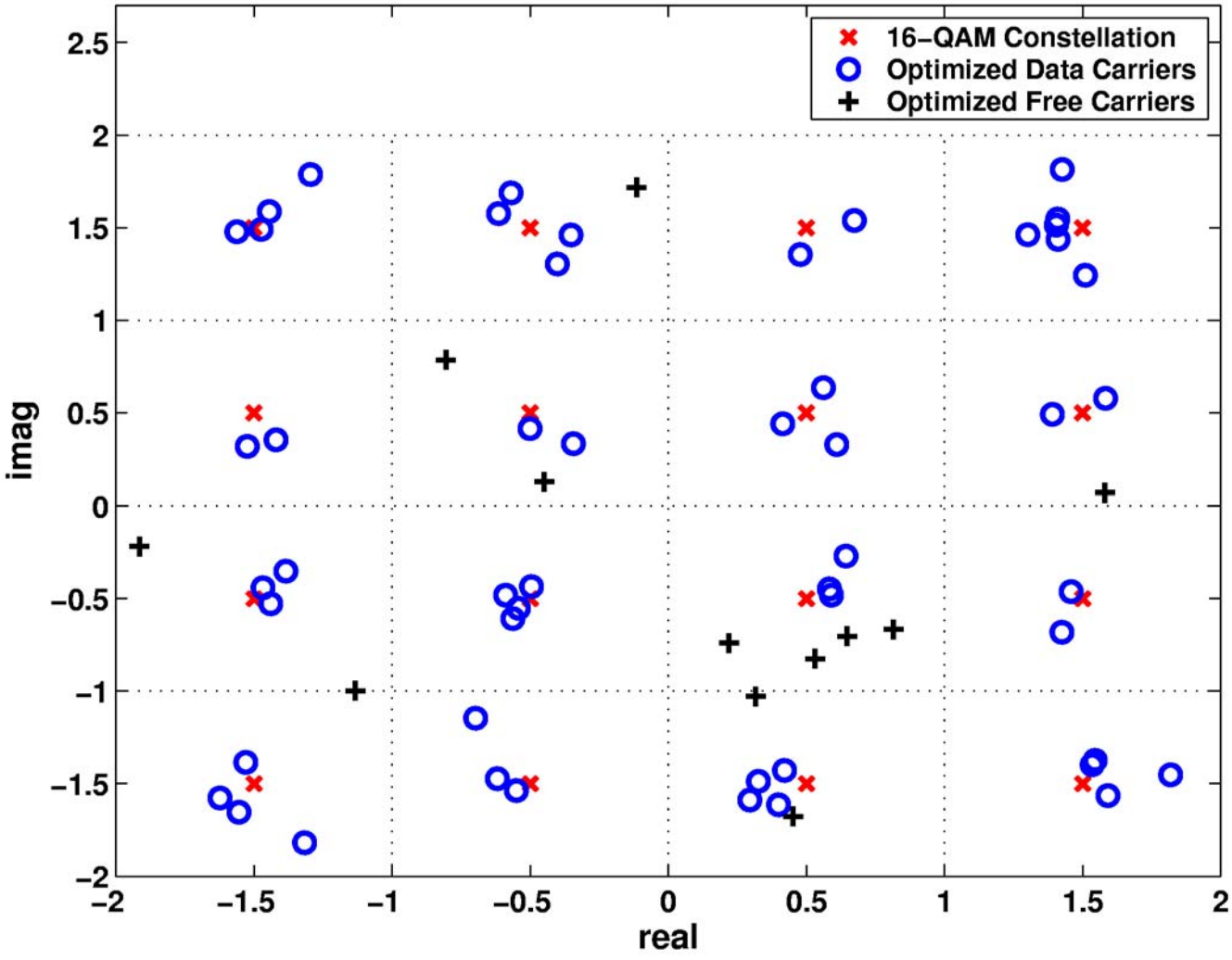
Example: Frequency-domain



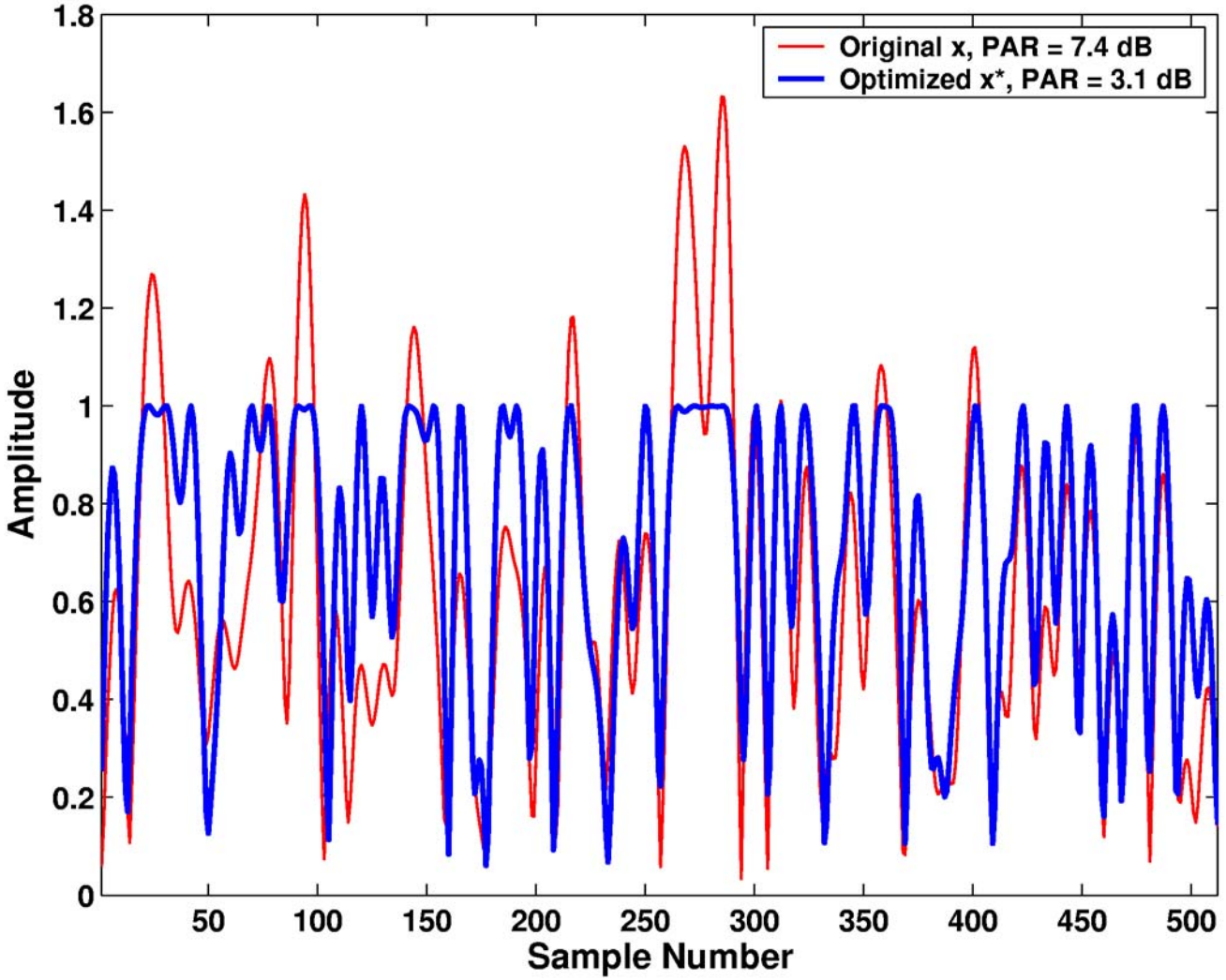
Example: Frequency-domain



Example: Frequency-domain



Example: Time-domain



Simulation Results: 802.11a/g

- Simulate 1000 random symbols for each data rate

Carrier Modulation	Maximum EVM (dB)	Original PAR μ (dB)	Original PAR σ (dB)	Optimized PAR μ (dB)	Optimized PAR σ (dB)
BPSK	-5	6.8	1.1	0.7	0.2
BPSK	-8	6.8	1.1	1.4	0.4
QPSK	-10	7.3	0.9	1.9	0.3
QPSK	-13	7.3	0.9	2.6	0.3
16-QAM	-16	7.3	0.9	3.1	0.4
16-QAM	-19	7.3	0.9	3.5	0.4
64-QAM	-22	7.3	0.9	3.8	0.5
64-QAM	-25	7.3	0.9	4.1	0.5

Convex Optimized PA

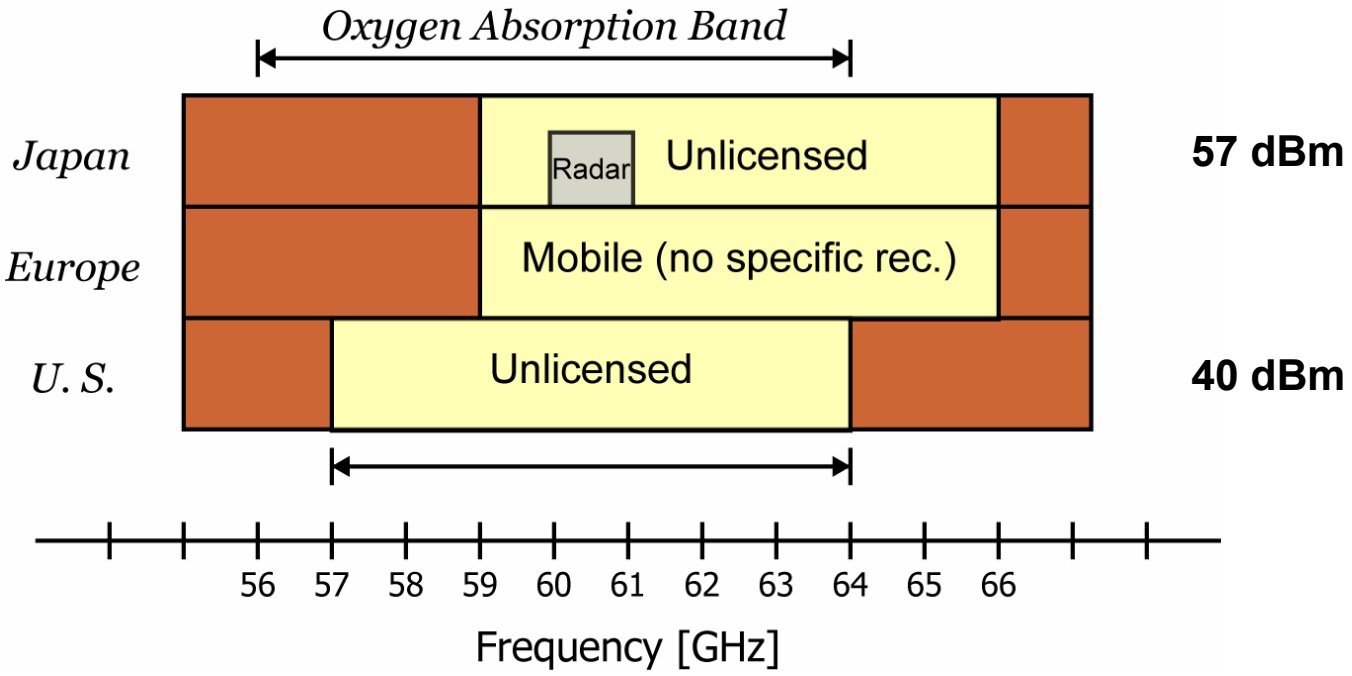
- Achieves globally minimum PAR in OFDM signals
- Delivers maximum power efficiency
- Establishes performance limits for analyzing existing PAR reduction methods
- Is feasible for real-time implementation using modern CMOS technology

Into the Future: Play on Antenna Gain

	5.15 - 5.25GHz	5.25-5.35GHz	5.470 -5.725GHz	5.725-5.825GHz
U.S.	40mW (Max) 160mW (EIRP) Indoor	200mW (Max) 800mW (EIRP) Indoor/Outdoor	200mW (Max) 800mW (EIRP) Indoor/Outdoor	800mW (Max) 160W (EIRP) Indoor / Outdoor
Europe	200mW (EIRP) Indoor		1W (EIRP) Indoor/Outdoor	25mW (EIRP) (5.725-5.875GHz)
Japan	200mW (EIRP) Indoor			

	Spectrum	Power	Antenna Gain
U.S.	2.4-2.4835GHz	1W	Like 5.725GHz
Europe	2.4-2.4835GHz	100mW (EIRP)	EIRP spec'ed
Japan	2.471-2.497GHz	10 mW/MHz	???

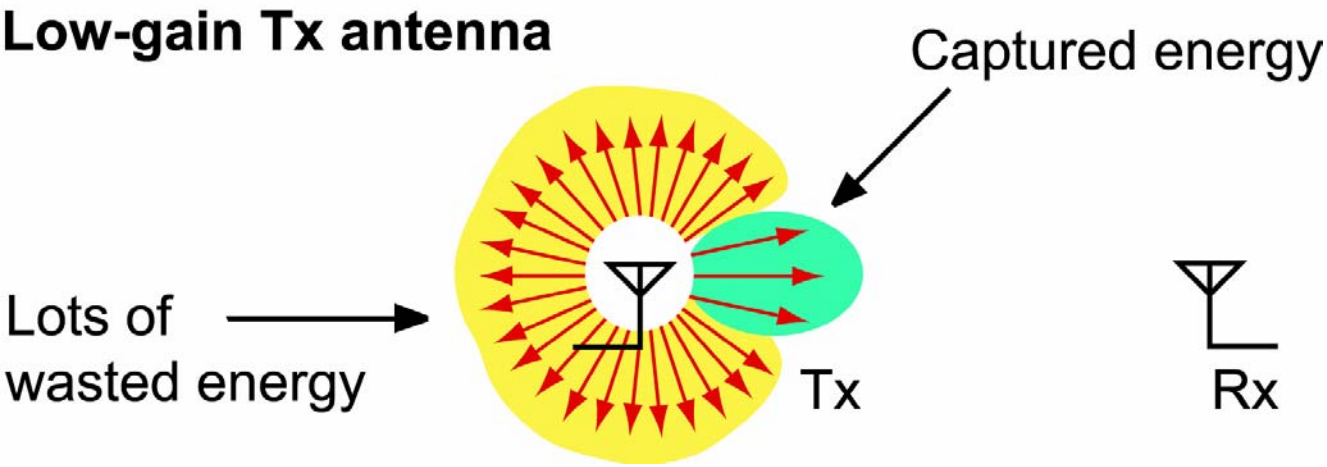
Why is 60 GHz interesting?



Lots of Bandwidth!!!

- 7 GHz of unlicensed bandwidth in the U.S. and Japan
- Reasonable transmit power (0.5W) and high antenna gains are allowed

Path Loss of Line-of-Sight



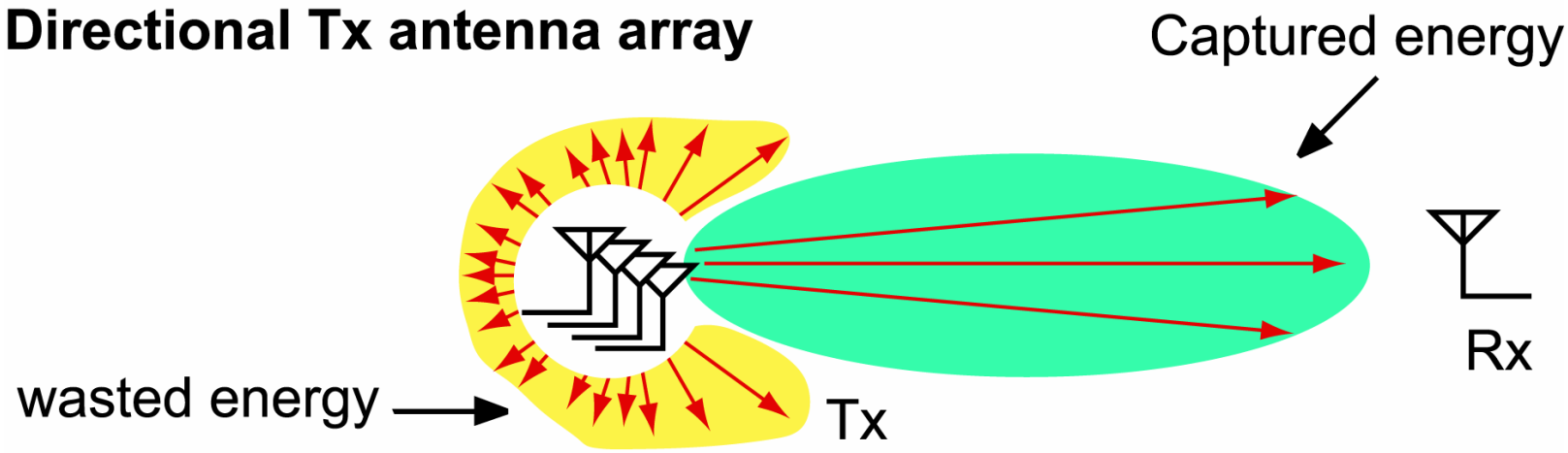
- Typical path loss (Friis) formula is a function of antenna gain Gr and Gt:

$$\frac{P_r}{P_t} = \lambda^2 \frac{G_r G_t}{(4\pi r)^2}$$

- But maximum antenna gain *increases with frequency* for the same antenna area, A

$$G = \frac{4\pi A}{\lambda^2}$$

Antenna Gain for Constant Area

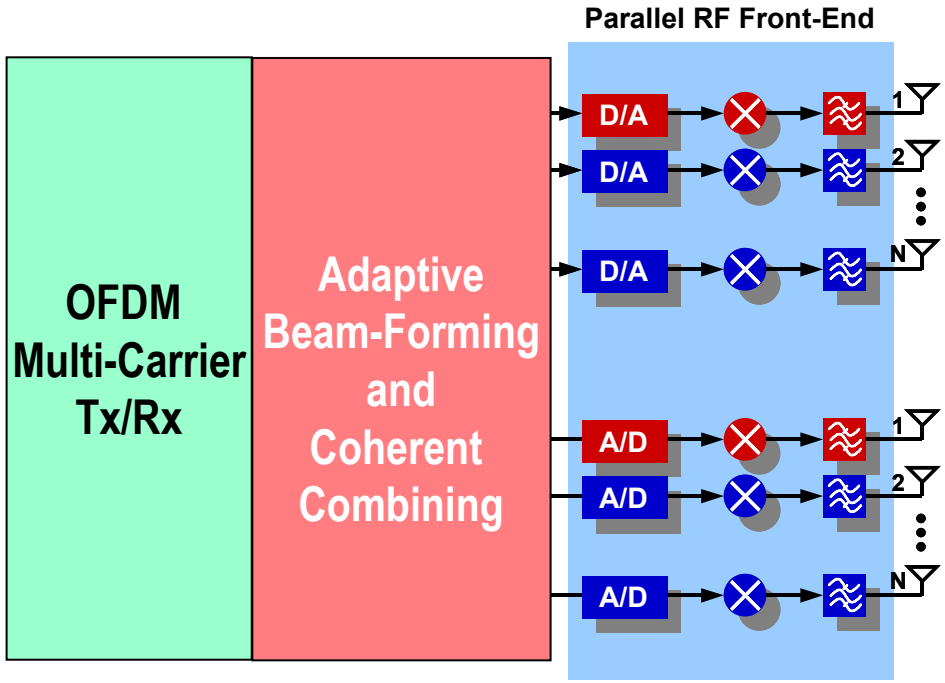


$$\frac{P_r}{P_t} = \frac{1}{\lambda^2} \frac{A_r A_t}{r^2}$$

- High carrier frequencies allow higher antenna gain with the same amount of antenna area
- There is theoretically 22 dB gain at 60 GHz over 5 GHz with optimal antenna design

Future SoCs: MIMO on a Chip

- **Goal:**
  - Multiple transmit/receive chains on a single chip
- **Challenges**
  - Complexity, crosstalk
- **Advantages**
  - Range extension
  - Capacity increase
  - Cost reduction by SoC



SoC Complexity and Feasibility

- Range extension determined by 800mW x 200 ~ 160 W!
- Capacity increase determined by the amount of diversity
  - 7 channels, 3 sectors, 20 transceiver chains per sector
  - 30Mbps for 20Mhz channel at 5Ghz, 1Gbps for 1Ghz channel at 60Ghz
  - Total capacity 7*3*(20/2)*30Mbps = 6.3 Gbps!
- Computation and silicon area requirements
  - Computation: 50 GOPS per transceiver, 7*3*20*50*2 GOPS = 42 TOPS
  - Digital silicon: 42,000 GOPS/1 GOPS/mm^2/4 ~ 10x10 cm^2
  - Analog silicon: 7*3*20*10 mm^2 ~ 7x7 cm^2
- At 60GHz, data rate is increased by another factor of 30.

Conclusions

- With highly energy efficient digital technology, we must challenge basic analog design techniques.
- Integration capability is crucial to future complex wireless system design.
- CMOS is able to exploit the unlicensed 60 GHz band with 7 GHz of bandwidth. However, it will take a new design and modeling methodology.
- Key to success: Interdisciplinary approach with device modeling, analog circuit design and DSP algorithms.

Thank you